REMARKS

By this amendment, independent claim 15 is canceled and replaced with claim 20 to place this application in condition for allowance. Currently, claims 16-20 are before the Examiner for consideration on their merits.

New claim 20 defines the wafer in terms of the processing sequence as previously claimed along with a limitation of low COPs and BMDs along an entire thickness of the wafer body. The surface density is defined after repeated Standard Cleaning -1.

In the rejection, the Examiner continues to assert that the heat treated wafer of Tamatsuka is indistinguishable from the wafer of the invention, whose structure is claimed after ingot growing and slicing but before the wafer has been subjected to any heat treatment. It is submitted that the wafer of the prior art does not anticipate the wafer as is presently claimed since the prior art wafer does not include, among other claim limitations, the combined low density of COPs and BMDs across the entire thickness of the wafer.

Turning back to the context of the invention, the wafer is intended for use in a particle monitor. While it is true that the intended use of the wafer cannot be used to distinguish the wafer itself, it is instructive for the Examiner to understand the makeup of the wafer for such an application and how this wafer makeup differs from the wafer produced by Tamatsuka.

For a wafer for use in a particle monitor, when the densities of COP and BMD in a thickness-wise direction become high, the number of particles increases at

subsequent device processing steps due to defects generated by the high densities of COPs and BMDs. This increase in particle numbers is on top of the particles which are generated due to the contamination during the device processing steps. Namely, when the density of COPs is high, the COPs grow into pits by the etching effects of the repeated cleaning so that these pits are detected as particles in addition to the genuine particles created in the device processing steps. This generation of pits in combination with the other particles aggravates the detection accuracy.

The high density of BMD causes these BMDs to precipitate on the wafer surface as crystal defects at a time when heat treatment is applied at the stage of the wafer inspection for contamination by particles before the device processing steps. Repeated cleaning renders these crystal defects to be detected as particles.

Because of the problems caused by high densities of COPs and BMDs, the inventors have discovered that controlling the growing of the single crystal wafer reduces the size and number of COPs in a pulling direction, which corresponds to the thickness direction of the wafers. This is accomplished by controlling a time period of passing the ingot through the temperature range from 1150 °C to 1070 °C to be within 20 minutes. The generation of BMDs is also suppressed through control of the processing of the ingot. When a time period for passing the ingot through the temperature range of 900 to 800 °C is controlled to be within 40 minutes, suppression of the generation of BMDs is achieved. The wafer, subjected to this controlled processing, is then sliced and no heat treatment is performed.

Comparing the inventive wafer as described above to Tamatsuka reveals that the Tamatsuka wafer is not the same as that now claimed. Tamatsuka relates to a wafer for use in devices having excellent intrinsic gettering capability. In these devices, a density of COPs having a size of 0.09 μm or more is 1.3 COPs/cm^2 or less in the surface layer ranging from the surface to a depth of 5 μm. It follows from this that the density of the COPs in the bulk portion of the wafer, i.e., other than the surface layer, is higher than the density in the surface layer.

In Tamatsuka, the wafer is not subjected to an ingot processing as used in the invention. Tamatsuka does engage in a specific heat treatment regimen wherein the wafer is subjected to a heat treatment under a non-oxidizing atmosphere at temperatures of 1100-1300 °C for 1 minute or more. The wafer is successively subjected to a heat treatment under an oxidizing atmosphere of 700-1300 °C for 1 minute or more. As a result of this heating sequence, a density of COPs in the surface layer can be reduced to form a high quality region suitable for device application. However, in the bulk portion, the density of COPs is kept high compared to that in the surface to thereby promote the formation of BMDs.

Each holding time for the non-oxidizing atmosphere heat treatment and the oxidizing atmosphere heat treatment is controlled to be short enough such as one hour maximum, see Examples 1 and 2, so that the nuclei for oxygen precipitation in the bulk portion won't disappear and can remain in it to thereby form BMDs with a sufficient density, while alloying the intrinsic gettering effects to be enhanced.

Meanwhile, Tamatsuka discloses that the cooling rate at the stage of pulling a single crystal is controlled to be 2.3 °C/minute or more in the temperature range of 1150-1080 °C, whereby the size and the number of COPs in a pulling direction are reduced. Nevertheless, the bulk portion of the wafer of Tamatsuka needs to be configured so as to have the larger number of COPs than that found in the surface layer to thereby promote forming BMDs. Because of the desire to have low COPs only on the surface of the wafer and higher densities in the bulk portion of the wafer to promote BMDs, when such a wafer is used for a particle monitor wafer, the BMDs precipitate on the wafer surface as crystal defects during heat treatment in device processing steps. Consequently, the number of particles to be generated in the device processing steps cannot be measured accurately.

The invention differs from Tamatsuka by the fact that density of COPs and BMDs along the entire thickness of the wafer body is reduced. Because of the reduction in the density of the BMDs, generation of defects attributable to the presence of BMDs can be prevented. Therefore and unlike the situation when considering the wafer of Tamatsuka, the number of particles to be generated in the device processing steps can be measured accurately. These differences can be seen in new claim 20, wherein the processing of the ingot is recited as well as the effect of such processing. That is, the claim requires that low density of COPs and BMDs occurs along the entire thickness of the wafer body and the surface density of particles of specified size is not more than 15 counts/cm^2 after repeated Standard Cleaning -1. Tamatsuka does not teach such a wafer and cannot be said to anticipate claim 20.

Moreover, since the inventive wafer and the wafer of Tamatsuka are fundamentally different, there is no basis from which to conclude that Tamatsuka could be used to formulate a rejection under 35 U.S.C. § 103(a).

Since claim 20 has been shown to be patentable over the applied prior art, its dependent claims 16-19 are also in condition for allowance.

Accordingly, the Examiner is respectfully requested to examine this application in light of this amendment and pass all pending claims onto issuance.

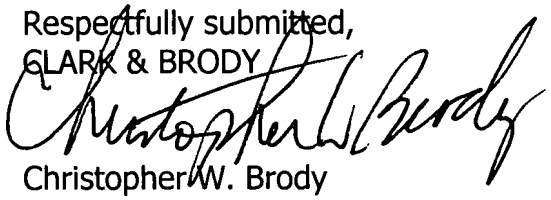
If the Examiner believes that an interview with Applicants' attorney would help expedite prosecution of this application, the Examiner is invited to telephone the undersigned at 202-835-1753.

The above constitutes a complete response to all issues raised in the outstanding Office Action of May 14, 2007.

Again, reconsideration and allowance of this application is respectfully requested.

Applicants petition for a three month extension of time. A check to cover the petition fee of $1,050.00 is enclosed. Please charge any fee deficiency or credit any overpayment to Deposit Account No. 50-1088.

Respectfully submitted,
CLARK & BRODY



Christopher W. Brody
Reg. No. 33,613

Customer No. 22902
1090 Vermont Ave. NW Suite 250
Washington, DC 20005
Telephone: 202-835-1111
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